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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,195	12/15/2003	Kwun Yao Ho	025796-00014	4785

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	**PAPER NUMBER**
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,195	HO ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed October 6, 2006.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4, 7, 11 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kong (U.S. 6,569,762).

4. Kong[1] (Fig. 1a-g) discloses: a multichip module structure, at least comprising: a first multichip module substrate, comprising: a semiconductor substrate (10; e.g. 35, Fig. 2a) having a first surface and a second surface (e.g. top and bottom); an insulating layer (12) on said first surface; a multilayer interconnection structure (13, 14, 15, 27) on said insulating layer and having a third surface (e.g. portion of dielectric, 16, beneath 15) having a plurality of first bonding pads (13) and a fourth surface (e.g. portion of dielectric beneath 27) having a plurality of second bonding pads (27) and on said insulating layer without contacting said semiconductor substrate (interconnect not physically touching substrate)[2]; a plurality of conductive plugs (23) penetrating through said semiconductor substrate and said insulating layer and electrically

[1] Alternatively, note that either Hoshino (U.S. 2002/0027293) or Bohr (U.S. 2002/0027293), which has been cited as pertinent art, could have been used to anticipate the claim in a similar manner.

connecting to said second bonding pads respectively; a plurality of third bonding pads (25) on said second surface and connecting to said conductive plugs respectively (e.g. Fig. 1g); and a plurality of chips (e.g. 34 and 33 stacked both on 35; Fig. 2a) formed on said second surface and electrically connecting to said third bonding pads;

(cl. 2) said multilayer interconnection structure includes at least one integrated circuit device (CLAIM 1 of Kong);

(cl. 4) where the chip is an active chip ("active area"; Col. 3, Line 44);

(cl. 7) where each of said chips electrically connect to third bonding pads (e.g. by plugs, Fig. 2a);

(cl. 11) where a second substrate is on the second substrate (e.g. 32 on second/ bottom surface of 33; Fig. 2a);

(cl. 12) with a packaged substrate on a third surface (e.g. 34 on third/ a part of top surface 33; Fig. 2a).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

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[2] Same basic structure as applicant's Figure 5

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kong (U.S. 6,569,762).

8. Kong discloses the elements stated in paragraph 4 and a thickness (e.g. layer is 3-dimensional) of its substrate, but fails to explicitly disclose that its thickness is 10 to 500 microns.

9. However, applicant has not disclosed that the dimensional selection was for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. As such, the selection of the dimensional limitation would have been obvious to one of ordinary skill in the art, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

10. Claims 5, 6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kong (U.S. 6,569,762) in combination with Juskey et al. (U.S. 6,356,453).

11. Kong discloses the elements stated in paragraph 4 of this office action and further a chip (33) mounted on the back of another chip (34) formed on the second surface (e.g. bottom of 35), but does not appear to explicitly show its chip being a passive or flip chip.

12. However Juskey (Fig. 5) utilize passive chips with active chips and flip chip.

13. It would have been obvious to one of ordinary skill in the art to form the chips in Kong as flip chip, passive and active chips in order to make device smaller, less expensive and faster devices as taught by Juskey (Col. 1, Lines 29-33; Col. 5-6, Lines 60-3).

14. With respect to the arrangement of the chips in claims 8-10 being a passive chip mounted on an active chip or visa versa, the operation of the device is not modified. As such, the rearrangement as claimed would have been obvious to one of ordinary skill in the art, since it has been held that mere shifting of parts was unpatentable absent evidence of where the rearrangement would not modify the operation of the device. See, In re Japikse, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

15. Claims 1-5, 7, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kong (U.S. 6,569,762) in combination with Hasimoto (U.S. 6,515,370)[3].

16. Kong (Fig. 1a-g) discloses: a multichip module structure, at least comprising: a first multichip module substrate, comprising: a semiconductor substrate (10) having a first surface and a second surface (e.g. top and bottom); an insulating layer (12) on said first surface; a multilayer interconnection structure (13, 14, 15, 27) on said insulating layer and having a third surface (e.g. portion of dielectric, 16, beneath 15) having a plurality of first bonding pads (13) and a fourth surface (e.g. portion of dielectric beneath 27) having a plurality of second bonding pads (27) and on said insulating layer without contacting said semiconductor substrate (interconnect not physically touching substrate)[4]; a plurality of conductive plugs (23) penetrating through said semiconductor substrate and said insulating layer and electrically connecting to said second bonding pads respectively; a plurality of third bonding pads (25) on said second surface and connecting to said conductive plugs respectively (e.g. Fig. 1g); and a chip (e.g. chip stack; Fig. 2a) formed on said second surface and electrically connecting to said third bonding pads;

(cl. 2) said multilayer interconnection structure includes at least one integrated circuit device (CLAIM 1 of Kong);

(cl. 4) where the chip is an active chip ("active area"; Col. 3, Line 44);

(cl. 7) chip connected third bonding pads;

(cl. 11) where a second substrate is on the second substrate (e.g. 32 on second/ bottom surface of 33; Fig. 2a);

(cl. 12) with a packaged substrate on a third surface (e.g. 34 on third/ a part of top surface 33; Fig. 2a).

17. Kong does not explicitly show a plurality of chips on said second surface or flip chips or the thickness of it substrate.

18. However, Hashimoto (Fig. 5, 6) teaches either the use of a single or a plurality flip chips connected to a bottom surface.

19. It would have been obvious to one of ordinary skill in the art to incorporate flip chips on the second /bottom surface of Kong in order to provide pitch conversion as taught by Hashimoto (Col. 9, Line 29-30), resulting in multi-chip modules with increased density and speed.

20. Furthermore, with respect to a plurality of chips, since the prior art already discloses a single chip formed on the bottom, to add an additional chip would result in mere duplication of a part without any new or unexpected result. As such, multiple chips in lieu of one would have been obvious[5], since it has been held that held that

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[3] Alternative interpretation, that each chip of said plurality of chips is in direct mechanical contact with the second surface.
[4] Same basic structure as applicant's Figure 5
[5] Those of ordinary skill in the art will understand at the time the invention was made that the device may contain duplication of parts (e.g. more than one chip). See for example, Hashimoto in Figures 5 and 6 that show its invention can either contain a single chip on its bottom surface or plurality of chips.

mere duplication of parts has no patentable significance unless a new and unexpected result is produced. See, In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

21. With respect to the thickness limitation of claim 3, Kong discloses a thickness (e.g. layer is 3-dimensional), but fails to explicitly disclose that its thickness is 10 to 500 microns. However, applicant has not disclosed that the dimensional selection was for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. As such, the selection of the dimensional limitation would have been obvious to one of ordinary skill in the art, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

22. Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kong (U.S. 6,569,762) and Hashimoto (U.S. 6,515,370) as applied to claim 1 and further in combination with Juskey et al. (U.S. 6,356,453).

23. Kong does not appear to explicitly show its chip being a passive chip.

24. However, both Hashimoto (Col. 16, Lines 13-21) and Juskey utilize passive chips with active chips.

25. It would have been obvious to one of ordinary skill in the art to form the chips in the modified structure of Kong as both passive and active chips as taught by Hashimoto in order to make device smaller and less expensive as taught by Juskey (Col. 1, Lines 29-33).

Response to Arguments

26. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D.
December 23, 2006

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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